

Fig. 1

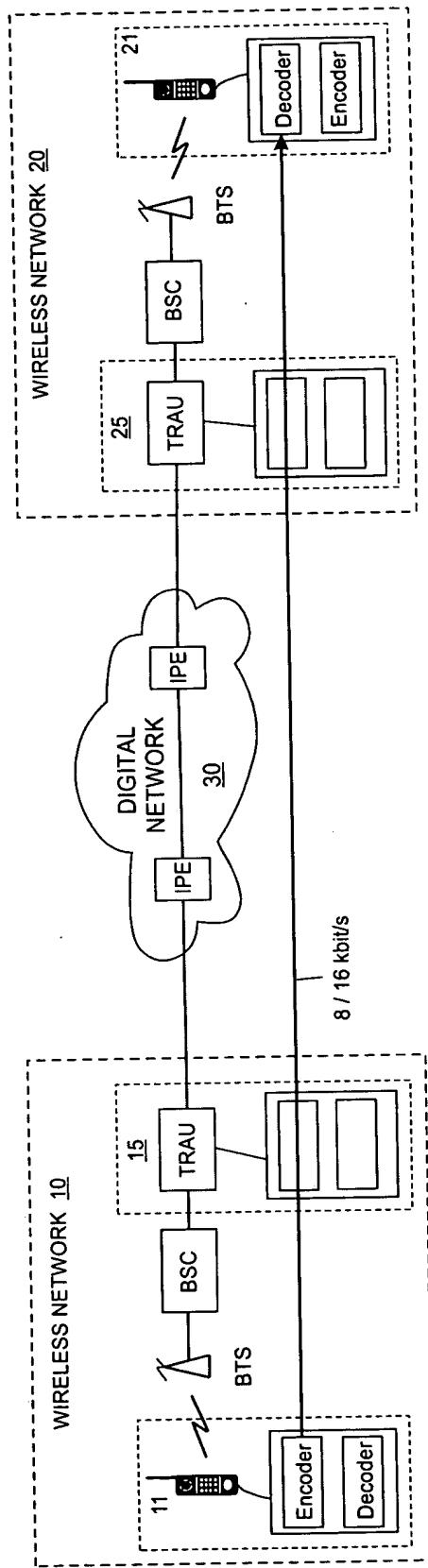
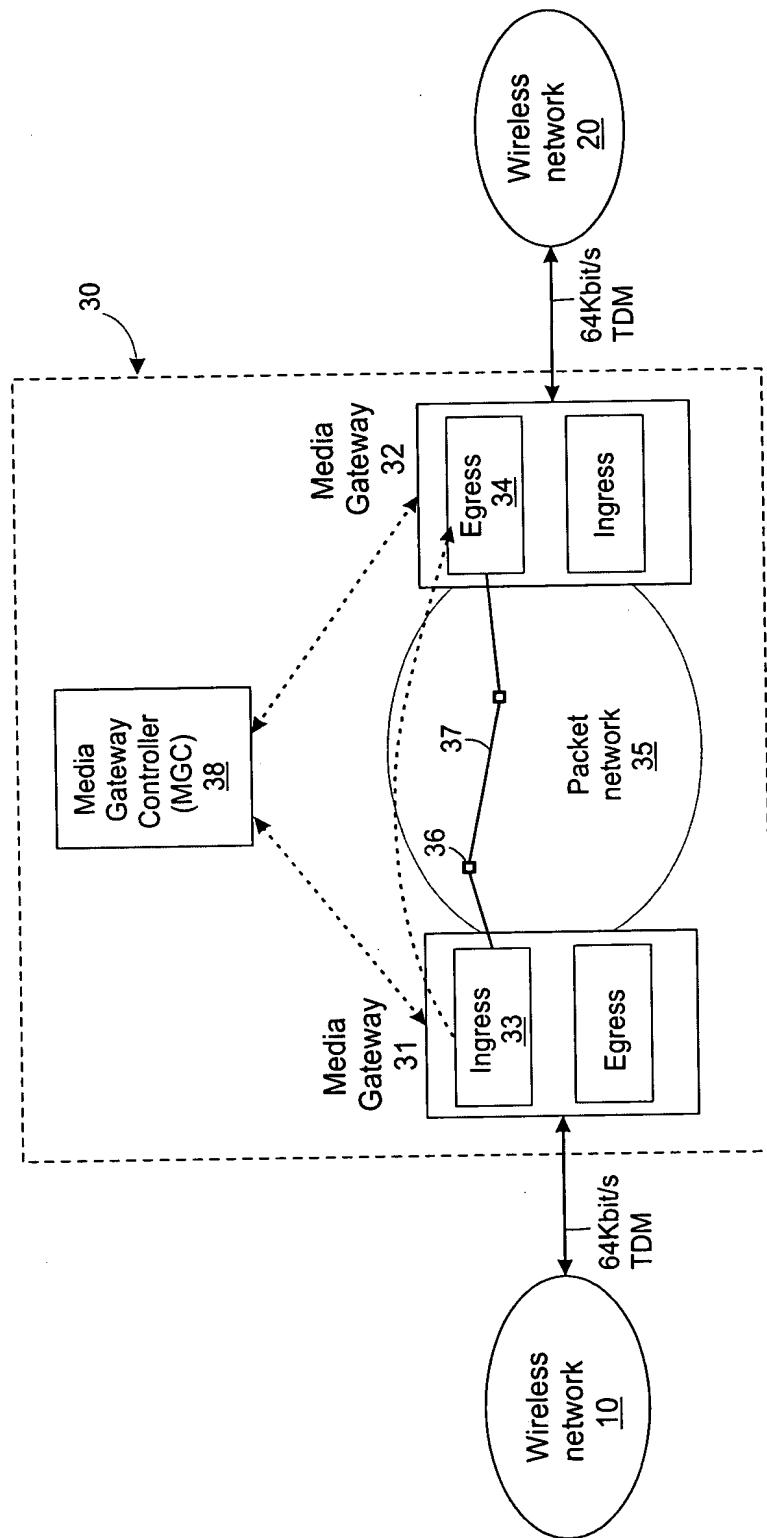
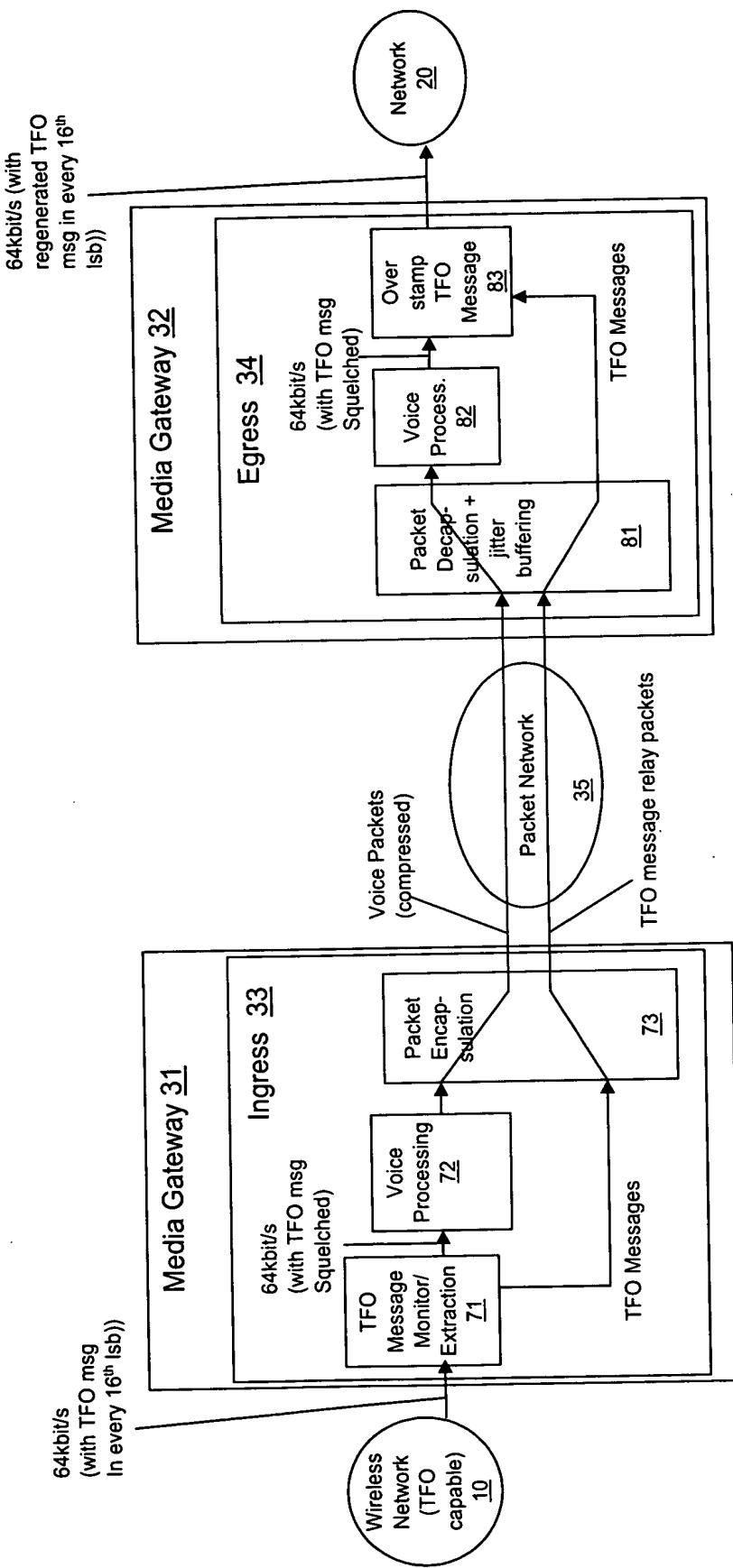


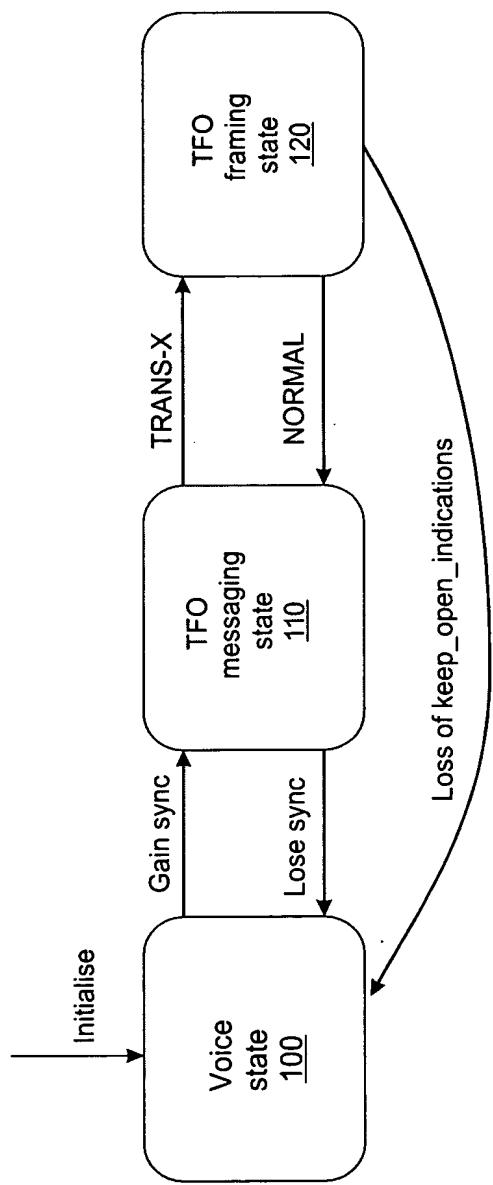
Fig. 2

**Fig. 3**

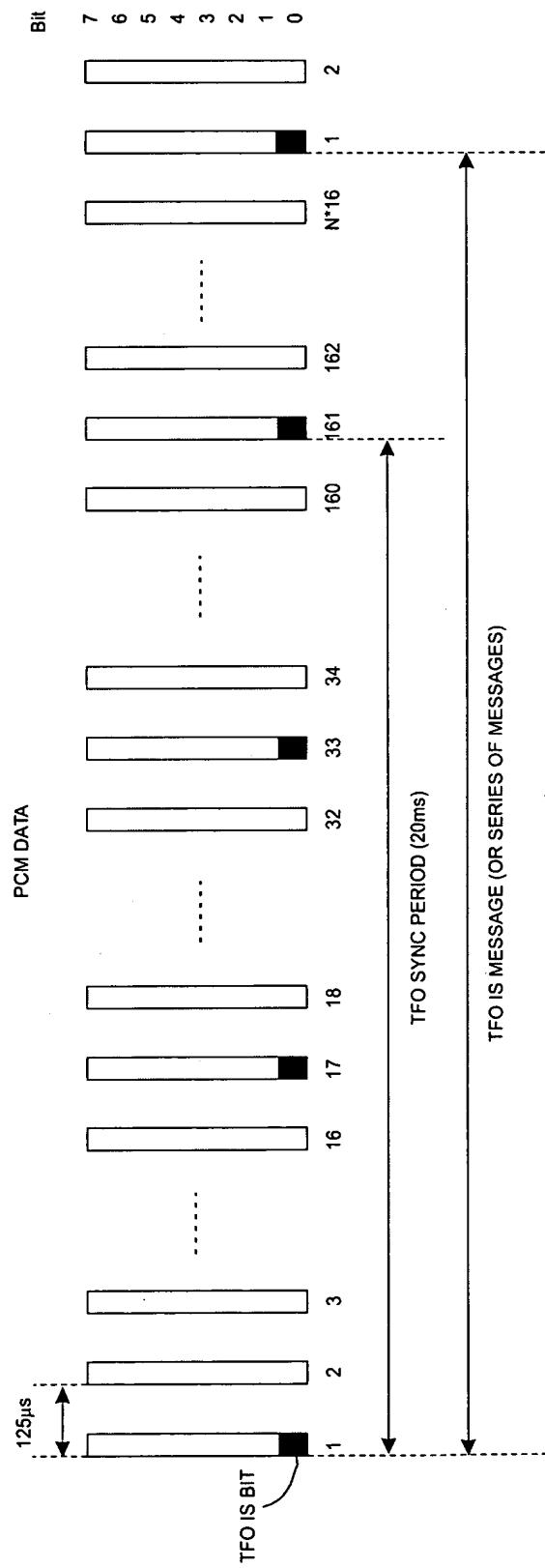


**Fig. 4**





**Fig. 5**



**Fig. 6**

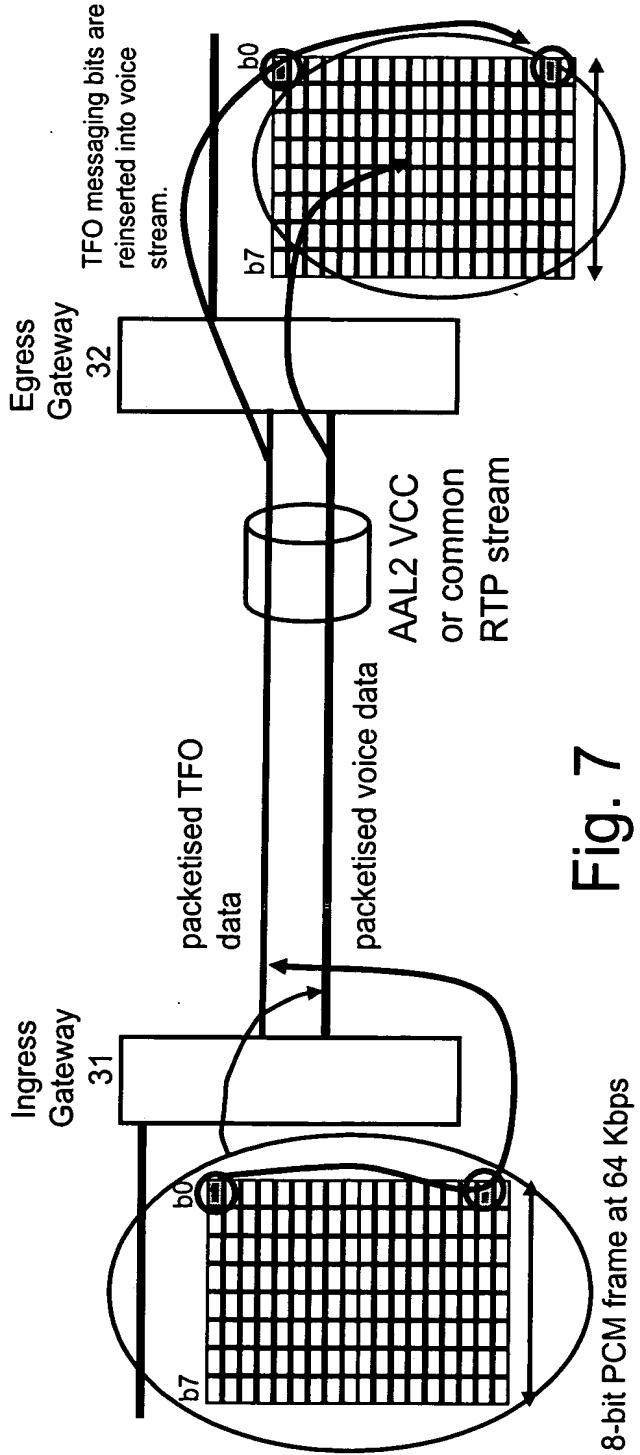


Fig. 7

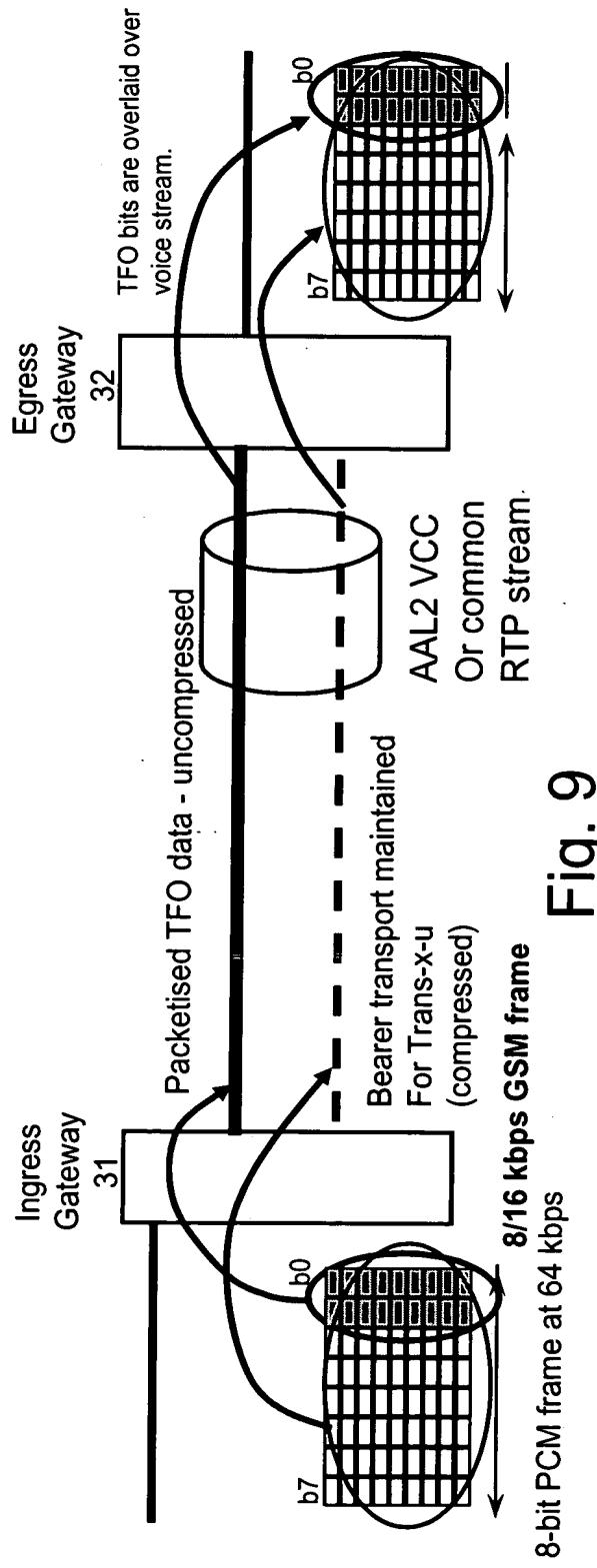
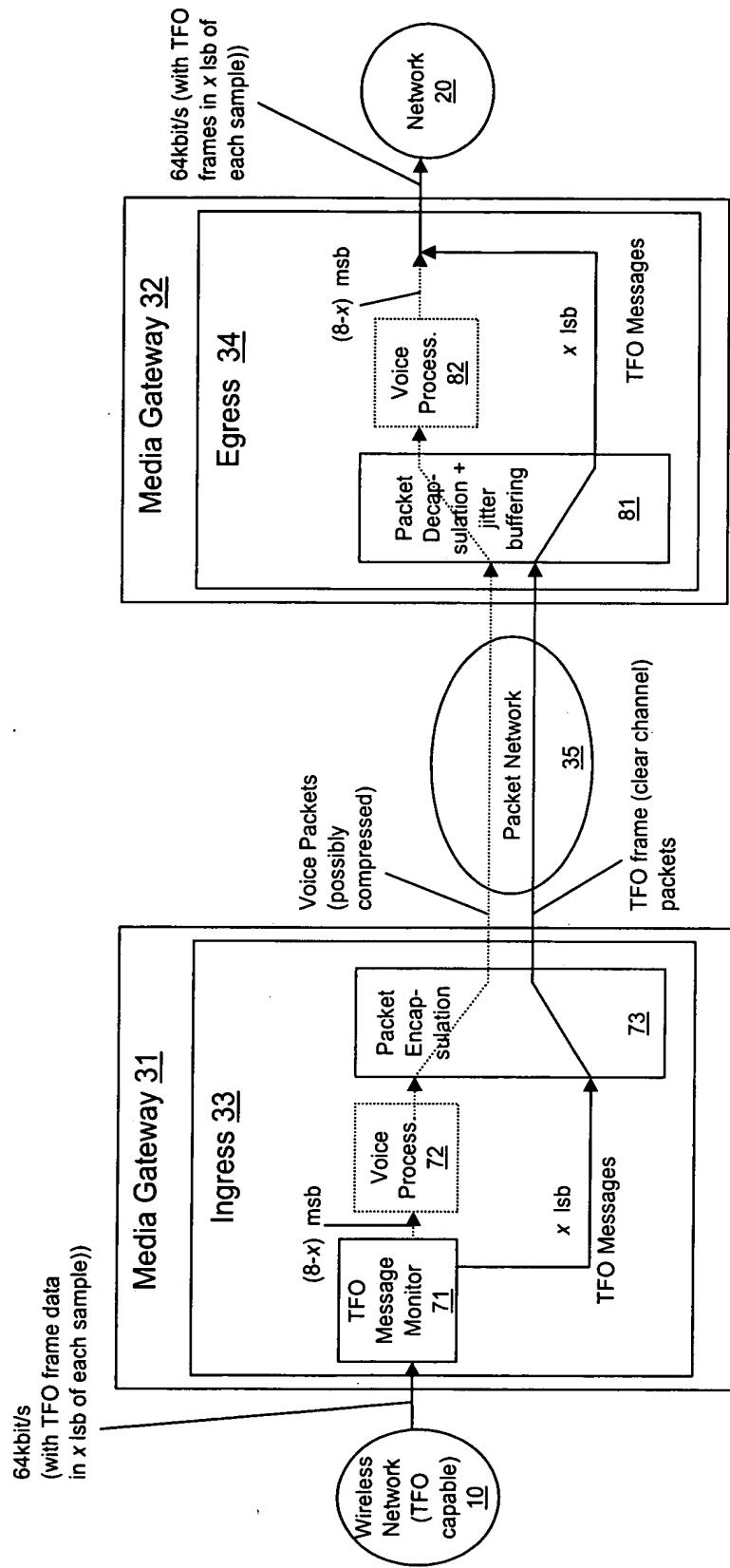


Fig. 9



**Fig. 8**

NOTE:  $1 \leq x \leq 8$

Byte	RES=0	Offset	Number of Bits	2	...	N
				TFO Message Fragment		(PAD=0)

Fig. 10A

0	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	
RES=0	Offset=0	No. Bits=10																					
			TFO Message Fragment																			PAD=0	

Fig. 10B

0	1	2	3	4	5	6	7
0	D						

Fig. 10C

0	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	
FO13	FO14	FO15	FO16	FO17	FO18	FO19	FO20	FO21	FO22	FO23	FO24	FO25	FO26	FO27	FO28								
FO29	FO30	FO31	FO32	FO33	FO34	FO35	FO36	FO37	FO38	FO39	FO40												PAD = 1

Fig. 10D

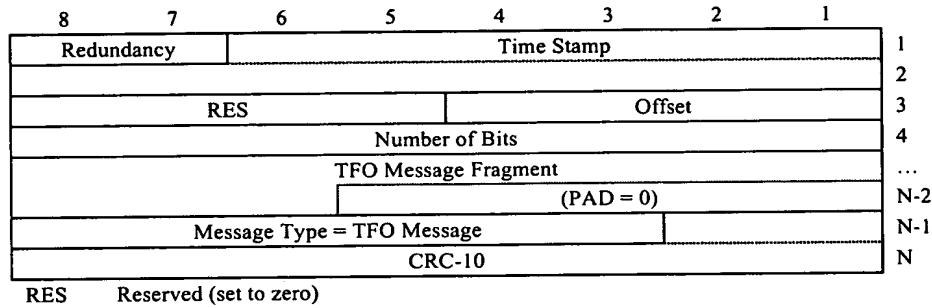


Fig. 11A

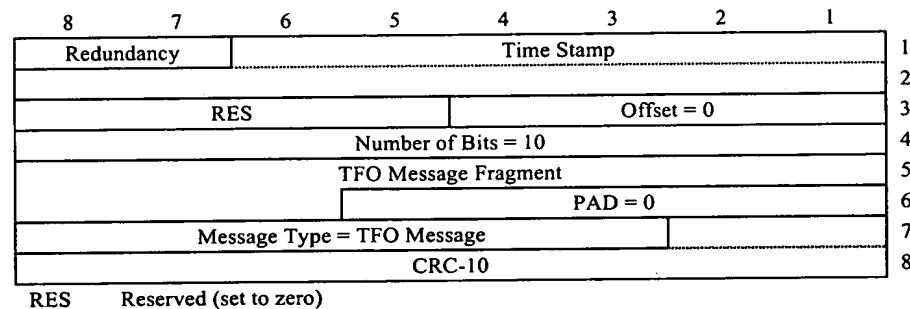


Fig. 11B

8	7	6	5	4	3	2	1	
FO 1	FO 2	FO 3	FO 4	FO 5	FO 6	FO 7	FO 8	1

**8 kbit/s circuit mode data EDU format**

8	7	6	5	4	3	2	1	
FO 1		FO 2		FO 3		FO 4		1
FO 5		FO 6		FO 7		FO 8		2

**16 kbit/s circuit mode data EDU format**

8	7	6	5	4	3	2	1	
FO 1			FO 2		FO 3			1
		FO 4		FO 5				2
FO 6		FO 7		FO 8				3

**24 kbit/s circuit mode data EDU format**

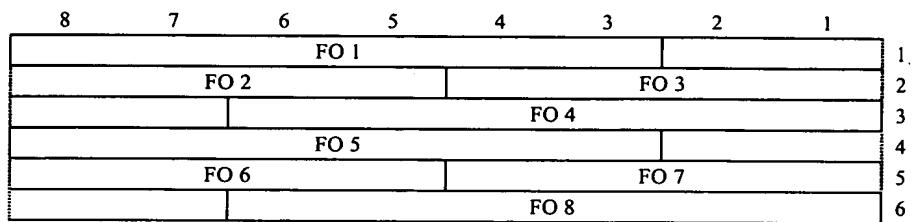
8	7	6	5	4	3	2	1	
FO 1				FO 2				1
FO 3				FO 4				2
FO 5				FO 6				3
FO 7				FO 8				4

**32 kbit/s circuit mode data EDU format**

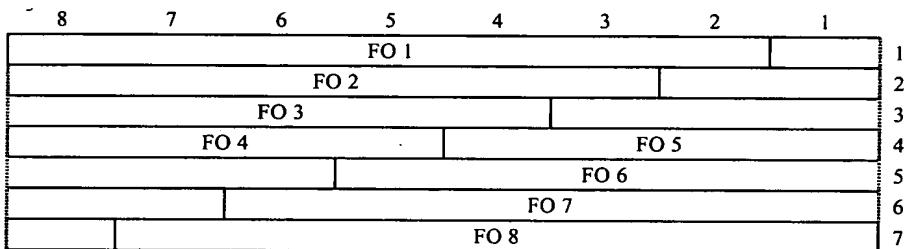
8	7	6	5	4	3	2	1	
FO 1				FO 2				1
			FO 3					2
		FO 4			FO 5			3
			FO 6					4
FO 7				FO 8				5

**40 kbit/s circuit mode data EDU format**

**Fig. 11C**



**48 kbit/s circuit mode data EDU format**



**56 kbit/s circuit mode data EDU format**

**Fig. 11D**